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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,906	06/09/2001	Hyeon-Seag Kim	M-11121 US	1914

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EXAMINER
OWENS, DOUGLAS W

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

P 5.

Office Action Summary	Application No.	Applicant(s)	
	09/877,906	KIM, HYEON-SEAG	
	Examiner	Art Unit	
	Douglas W Owens	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-9 and 11-28* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☒ Claim(s) *22-28* is/are allowed.

6)☒ Claim(s) *4,11-13,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent. No. 6,373,114 to Jeng et al.

Regarding claim 20, Jeng et al. teaches a semiconductor device formed on a substrate and comprising:

a channel region of first conductivity type (inherent feature of a MOSFET);

a dielectric layer (54) overlying the channel region;

a diffusion barrier layer (58) directly overlying the dielectric layer, said diffusion barrier layer being a single layer;

a gate electrode (60) directly overlying the diffusion barrier layer, said gat electrode layer comprising a semiconductor material (Col. 5, lines 49 – 52 (WSi_x));

a blocking layer (62) overlying the gate electrode; and

two source/drain regions of second conductivity type formed on opposite sides of the channel region (inherent feature of MOSFET).

Jeng et al. does not teach forming the MOSFET over a well region. The use of well regions in the formation of MOS transistors is well known in the art. It would have been obvious to one of ordinary skill in the art to incorporate a well region since it is

desirable for a channel region to form between the source and drain. For example, forming a p-channel transistor in p-type silicon would result in a device that is little more than a wire if a well region (n-type) is not incorporated into that device.

Regarding claim 4, Jeng et al. teaches a device, wherein the diffusion barrier layer and the blocking layer comprise silicon.

1. Claims 11 – 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,353,249 to Boyd et al.

Regarding claim 21, Boyd et al. teaches a semiconductor device (Fig. 1G, for example) formed on a substrate (10), comprising:

a channel region (38) of first conductivity type;

two silicon germanium filled spaces (34; Col. 4, lines 57 – 60);

a dielectric layer (26) overlying the channel region; and

a gate electrode (28) overlying the dielectric layer;

wherein the two silicon germanium filled spaces comprise source/drain regions (34) of second conductivity type on opposite sides of the channel region, wherein the source/drain regions comprise silicon germanium (Col. 4, lines 57 – 60).

Boyd et al. does not explicitly teach a well region. The use of well regions in the formation of MOS transistors is well known in the art. It would have been obvious to one of ordinary skill in the art to incorporate a well region since it is desirable for a channel region to form between the source and drain. For example, forming a p-channel transistor (as required in CMOS technology) in p-type silicon would result in a

device that is little more than a wire if a well region (n-type) is not incorporated into that device.

Regarding claim 11, Boyd et al. teaches a device, wherein the gate electrode comprises a metal (Col. 6, lines 49 – 52).

Regarding claim 12, Boyd et al. does not teach a semiconductor device, wherein the junction depth of the source/drain region is in the range of 100 to 1000 Angstroms. Boyd et al. is silent with respect to the junction depth of the source/drain regions. Therefore, one having ordinary skill in the art would have been required to arrive at the optimal junction depth through routine and obvious experimentation. It has been held that it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 13, Boyd et al. does not teach a device, wherein the source/drain region is formed in amorphous material. Boyd et al. does not specify the crystalline structure of the substrate. It would have been obvious to one of ordinary skill in the art to select amorphous silicon germanium since Boyd suggests the use of silicon germanium. Additionally, amorphous silicon germanium would have been well suited for the intended use.

Allowable Subject Matter

2. Claims 22 – 28 are allowed.

3. Claims 2, 3 and 5 –9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not teach a device as recited in claim 22, particularly, including epitaxial dielectric, diffusion barrier and blocking layers.

Response to Arguments

5. Applicant's arguments filed March 10, 2003 have been fully considered but they are not persuasive.

The Applicant argues that Jeng et al. does not teach "a diffusion barrier layer directly overlying the dielectric layer, said diffusion barrier layer being a single layer" and "a gate electrode directly overlying the diffusion barrier layer, said gate electrode layer comprising a semiconductor material."

Fig. 7 of Jeng et al. illustrates a diffusion barrier layer (58; Col. 4, lines 46 – 53), positioned such that it is directly overlying the dielectric layer. The term "directly overlying" is understood to mean that the diffusion barrier layer is not obliquely positioned above the dielectric layer. The term does not necessarily require that the diffusion barrier layer be in direct contact with the dielectric layer, only that the diffusion barrier layer overlies the dielectric layer, but not obliquely. Additionally, as discussed in lines 46 – 53, Col. 4 of Jeng et al., the barrier layer (58) comprises one layer.

With respect to the gate electrode comprising a semiconductor material, Jeng et al. discloses this feature in lines 49 – 52 of column 5, where it is taught that the gate electrode is tungsten silicide, which inherently includes silicon (WSi_x), a semiconductor material. While Jeng et al. does disclose that the gate includes a metal, the broad claim

language does not preclude metal from being incorporated into the gate as long as a semiconductor material is present.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DWO
May 15, 2003

Steven Loke